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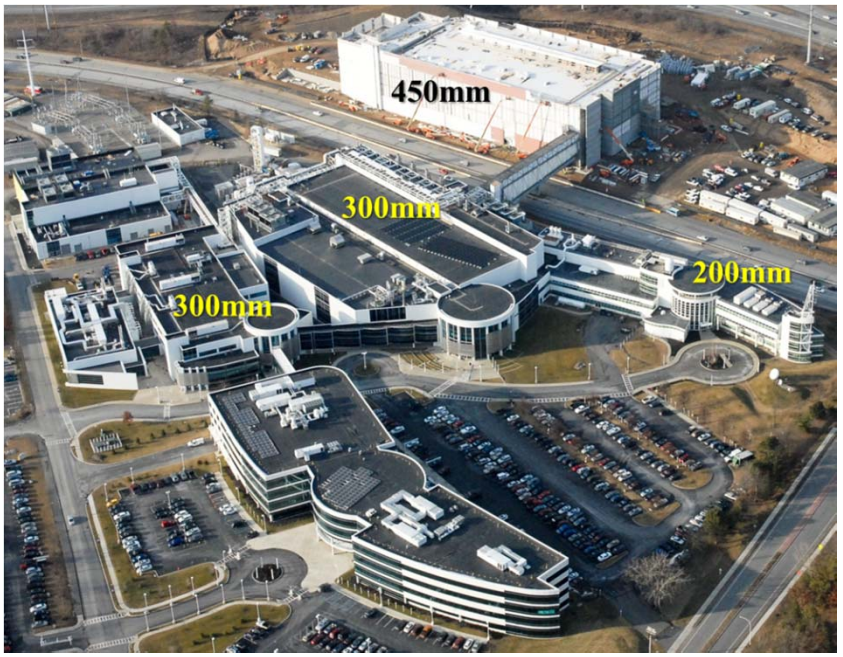
Scaling Options in Relation to 450mm

October 8, 2014

WWW.SUNYCNSE.COM

Agenda

- Introduction
- Lithography
- 450 mm
- 3Di/Packaging
- Other semiconductors



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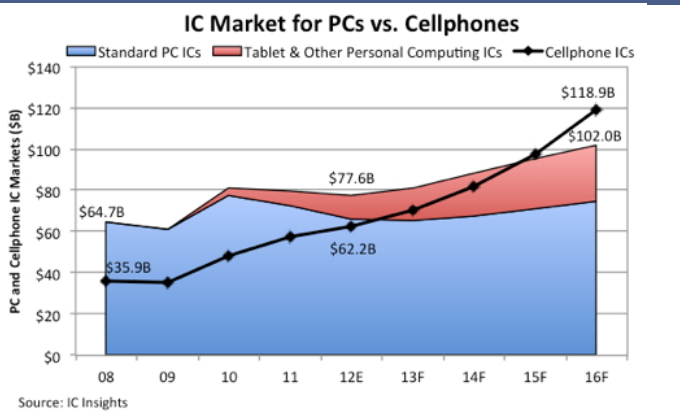
Environment

- **Smart phones surpass PCs in chip sales**



- **Leading-edge industry consolidation**
  - Foundries; IDMs
  - Equipment suppliers

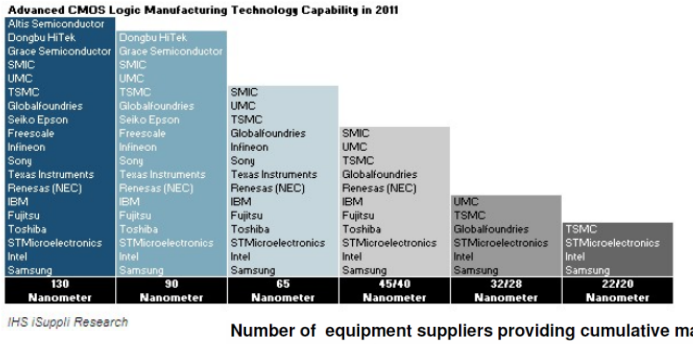
- **How far/fast will scaling continue?**
  - Continued scaling is cost driven

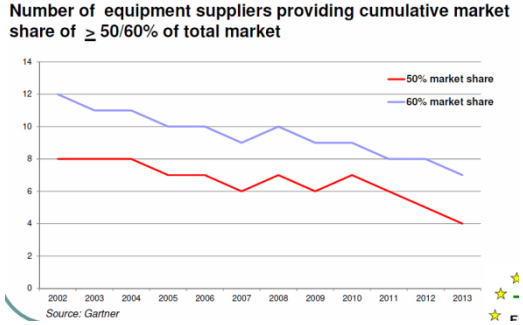
(A.Manocha; Semicon West 2013)

Based On SRAM Size & Other Information Seen In Our Consulting Work, In Our View The "14nm" Nodes From Each Manufacturer Should Be Called:

- Intel – 16nm or 17nm
- Samsung – 18nm
- TSMC & GF – 20nm
- STM – 21nm

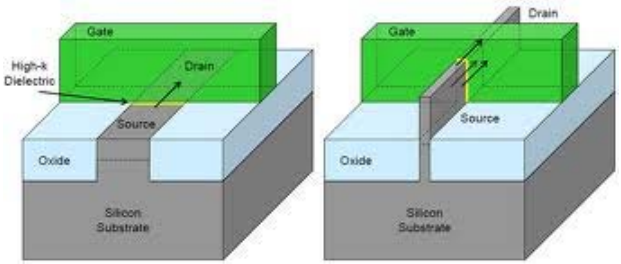
(Future Horizons, Semicon Europa 2013)



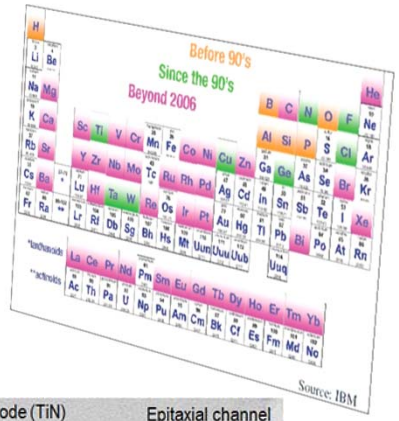


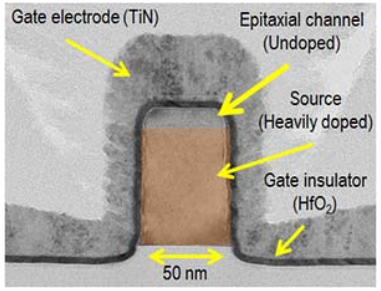
How can Moore's Law be extended?

- **Performance / Power Consumption**
  - New materials
  - New devices
  - New architectures



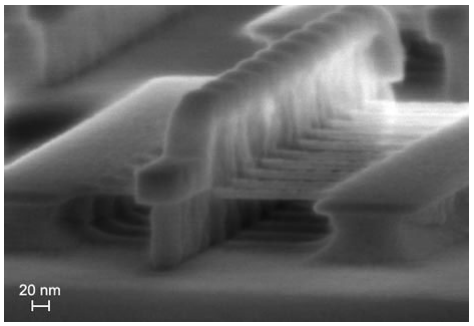
www.semiwiki.com





http://phys.org/news

- **Cost**
  - Lithographic scaling
  - Wafer size scaling
  - Chip stacking "3D"



http://spectrum.ieee.org

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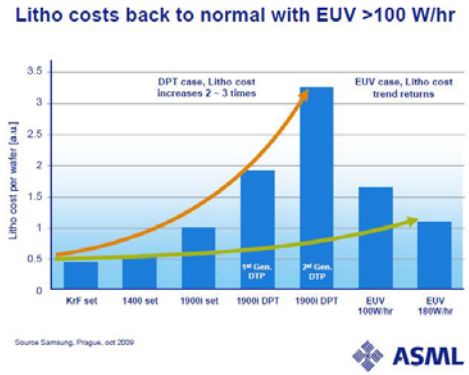

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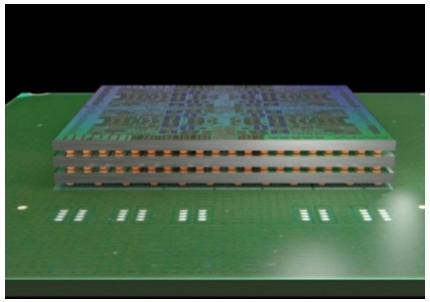
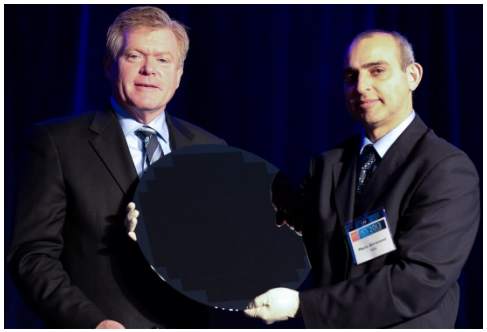


http://ibmresearchnew.blogspot.com



http://450mm.com

Agenda

- Introduction
- **Lithography and materials**
- 450 mm
- 3Di/Packaging
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CNSE Albany Silicon Capabilities

- Full complement of 300 mm wafer tools
  - ✓ Leading-edge lithography
  - ✓ Backwards compatible to 65 nm; license
- Used today for 10-7 nm CMOS development
  - ✓ CNSE is a joint development partner
- Capacity of ~30 integrated wafer starts per day
  - ✓ 24/7 operation
- 1st 450mm tool set in the industry

ST
SAMSUNG
IBM
GLOBALFOUNDRIES

TEL
TEL

APPLIED MATERIALS

Lam RESEARCH

ASML

SEMATECH

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Lithography Industry Challenges

- 193nm Cannot Meet Requirements for Scaled “7nm”
- 10nm Uses Patterning Tricks to Extend 193 Capability
  - Smaller CD but increasingly complex
    - Multiple-Pass Litho / Litho-Etch-Litho-Etch — ↑ Complexity
    - Self-Aligned Double Patterning (Sidewall Image Transfer) — ↑ Variability
    - Source Mask Optimization Restrictions — ↑ Design Limits
- EUV Is Simpler and *Potentially* Cheaper @ 7nm Node
  - Min Feature Size ~15nm
  - Simplified Patterning
    - Single-Pass Litho Reduces Mask Count — ↓ Variability
    - Single SIT Processes — ↓ Complexity
    - Wider Process Window — ↓ Defectivity
    - Bi-Directional Printing Possible — ↓ Design Limits

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EUV Lithography Program

EUV is gated by scanner productivity

- A throughput of above 100 wafers/hr. is considered sufficient

Other key infrastructure items

- Actinic defect inspection (SEMATECH EMI program)
- Mask blank development (SEMATECH mask blank center)
- Resist Enablement Center access to MET and EUV full field
- Mask pellicle need / development

ASML 3300
at CNSE

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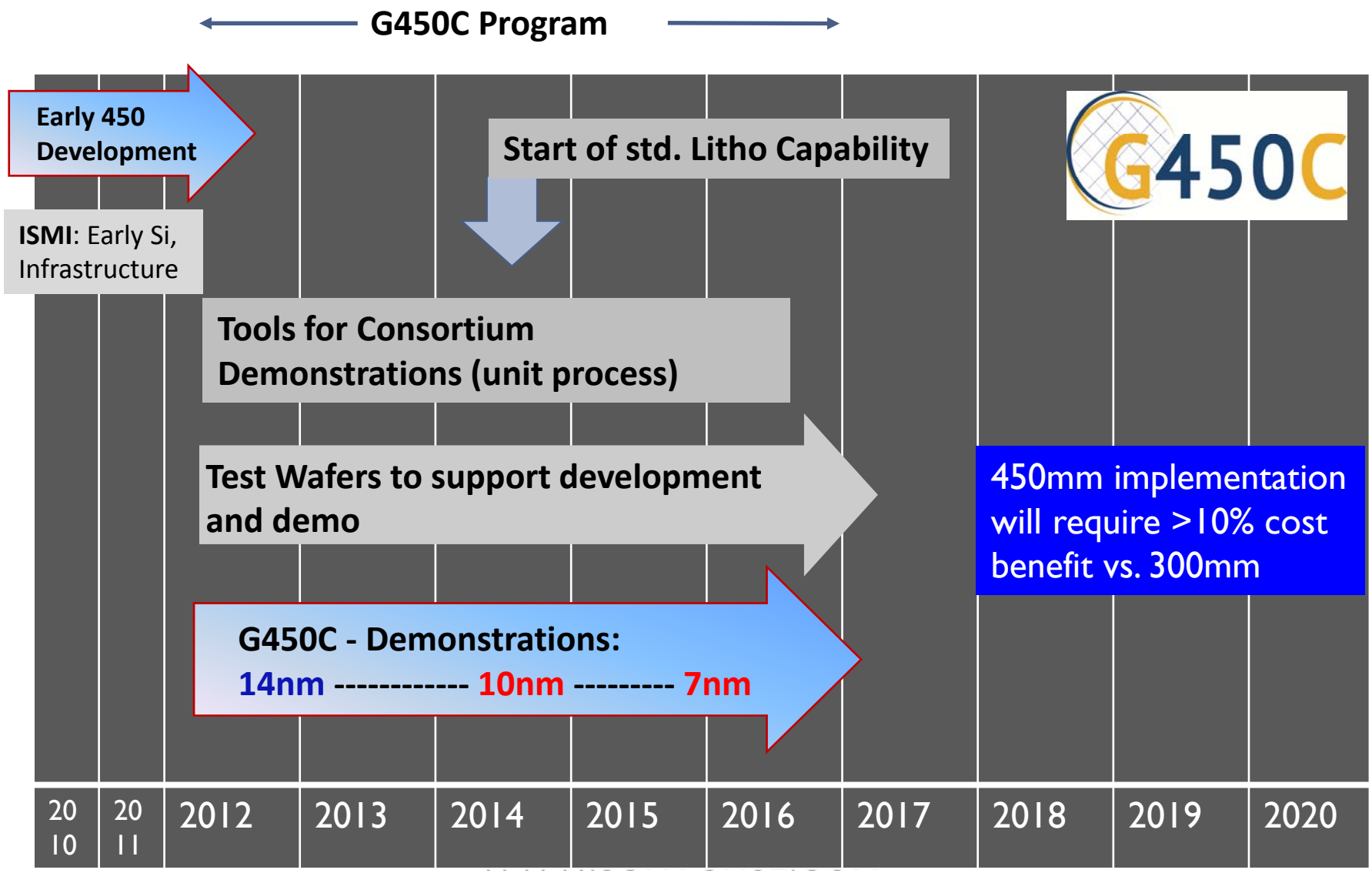
Development and Technology Intercept Targets



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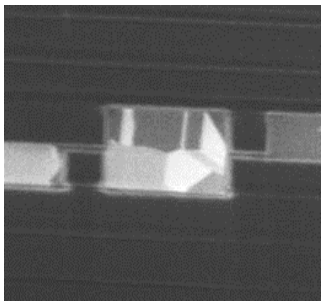
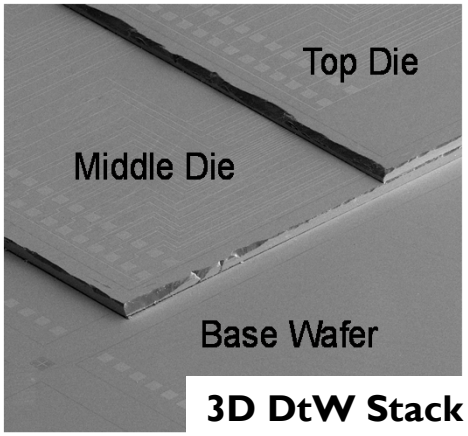
3D Integration @ CNSE

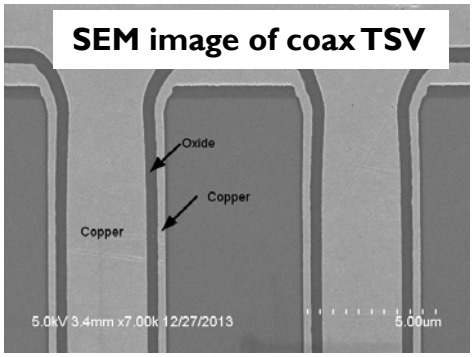
- Full 2.5D/3D integrated process developed and implemented
- 3D DtW and WtW bonding
- Mid-via integration in 65 nm CMOS
- Fully customer tape-out ready

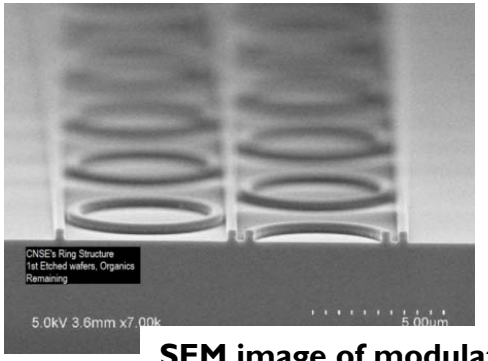




3D DtW Stack

- Currently used, e.g., for integrated photonics on interposer





SEM image of modulator

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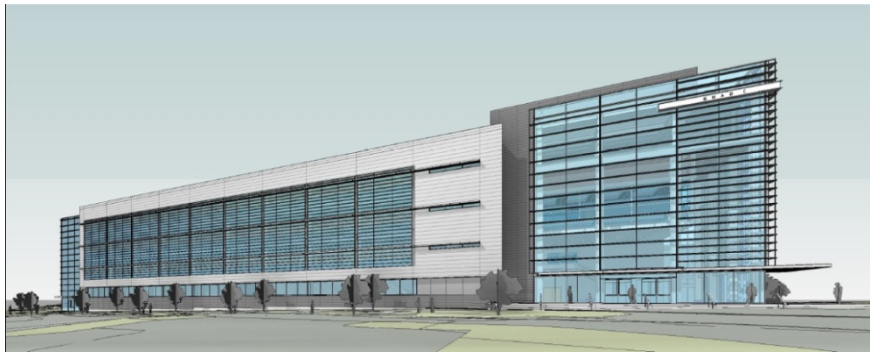
3Di Manufacturing Utica NY – SUNY IT

- **NYS Funded Packaging Facility**
  - RFE 10/15/2014

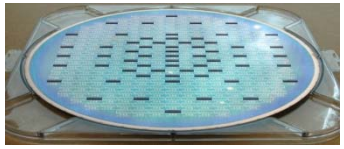


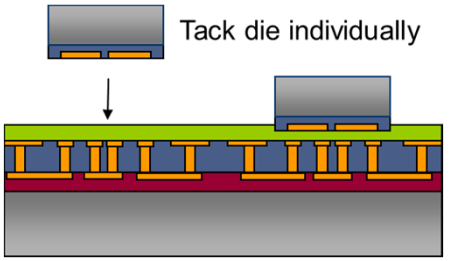
- **Technology Center for Standard and Advanced Packaging Manufacturing**
  - Provide packaging R&D consortia option for companies to interact and develop business opportunities
  - Offer quick turn facility for customer packaging applications

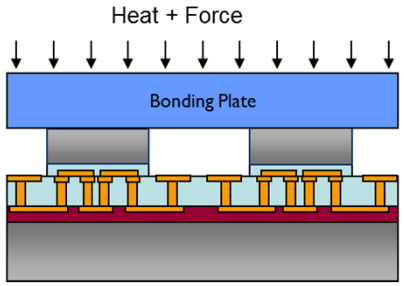
South West Corner

Key Challenges – Cost and Control

- **Top three process and equipment-related issues in 3D:**
  1. ***Cost***
  2. ***Cost***
  3. ***Cost***
  4. No standards







- **Die-Wafer**
  - Speed of die attach process / tooling
  - Die level tracking
  - Process control
- **Wafer-Wafer**
  - KGD – test and overall yield
  - Die size matching
- **Alternatives?**

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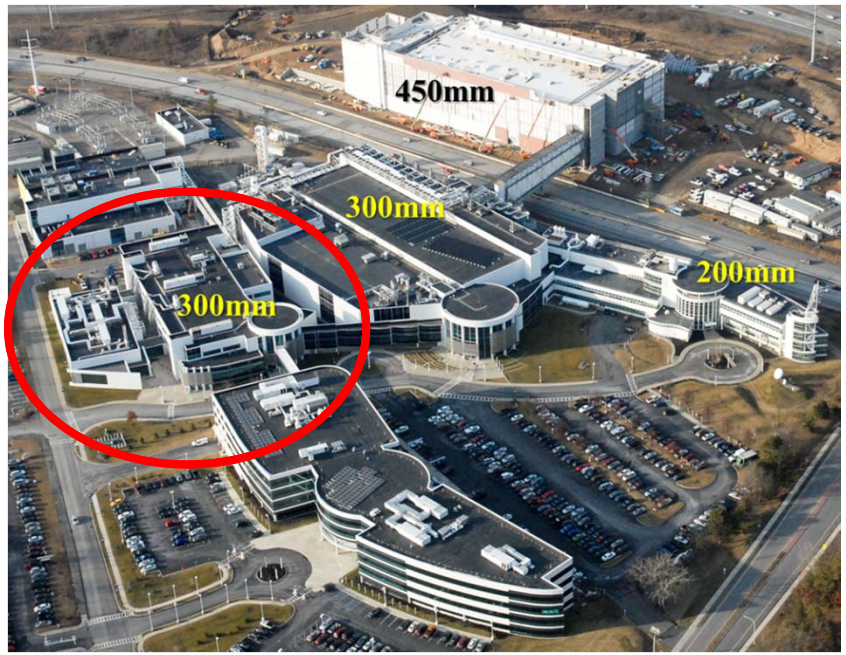

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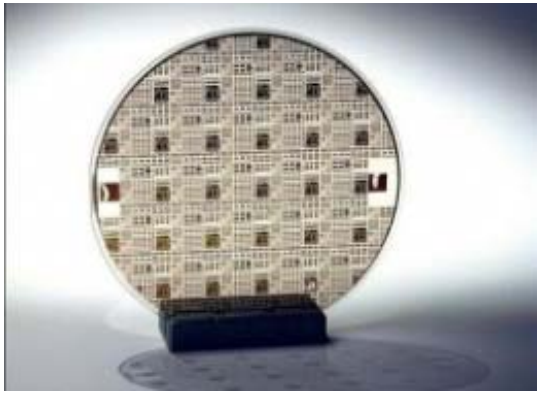
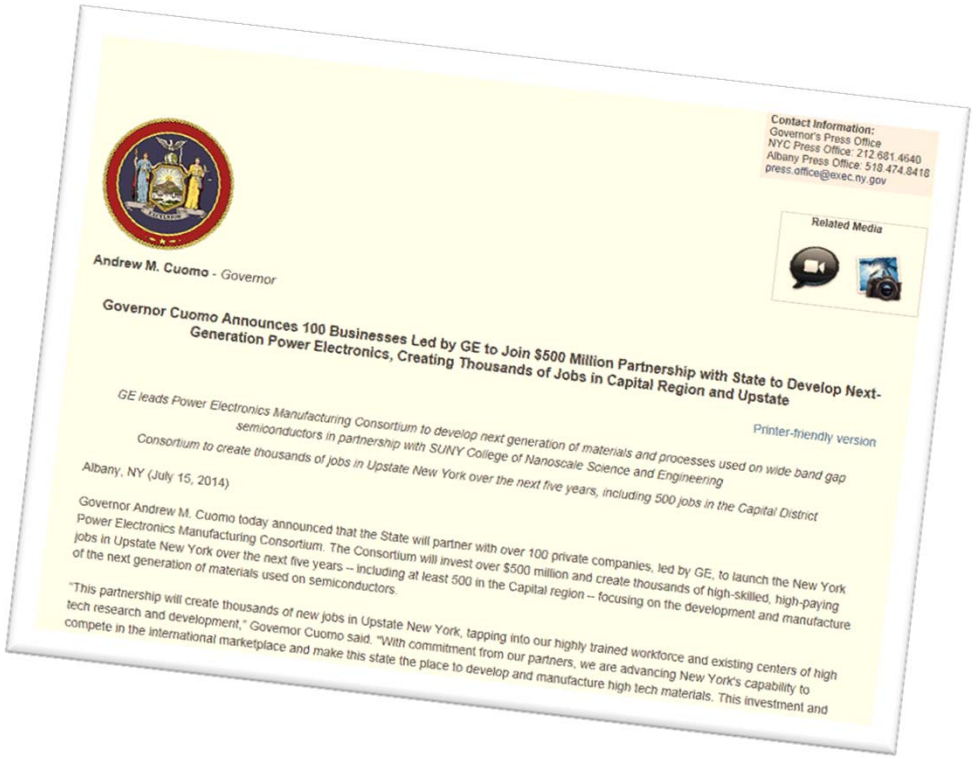
NEW YORK POWER ELECTRONICS MANUFACTURING CONSORTIUM

imagination at work





Contact Information:
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NYC Press Office: 212.681.4640
Albany Press Office: 518.474.8418
press.office@exec.ny.gov

Related Media

Andrew M. Cuomo - Governor

Governor Cuomo Announces 100 Businesses Led by GE to Join $500 Million Partnership with State to Develop Next-Generation Power Electronics, Creating Thousands of Jobs in Capital Region and Upstate

Printer-friendly version

GE leads Power Electronics Manufacturing Consortium to develop next generation of materials and processes used on wide band gap semiconductors in partnership with SUNY College of Nanoscale Science and Engineering

Consortium to create thousands of jobs in Upstate New York over the next five years, including 500 jobs in the Capital District

Albany, NY (July 15, 2014)

Governor Andrew M. Cuomo today announced that the State will partner with over 100 private companies, led by GE, to launch the New York Power Electronics Manufacturing Consortium. The Consortium will invest over $500 million and create thousands of high-skilled, high-paying jobs in Upstate New York over the next five years -- including at least 500 in the Capital region -- focusing on the development and manufacture of the next generation of materials used on semiconductors.

"This partnership will create thousands of new jobs in Upstate New York, tapping into our highly trained workforce and existing centers of high tech research and development," Governor Cuomo said. "With commitment from our partners, we are advancing New York's capability to compete in the international marketplace and make this state the place to develop and manufacture high tech materials. This investment and

Initial fab capacity 10k wafers/yr
Total fab output up to 1TVA/yr

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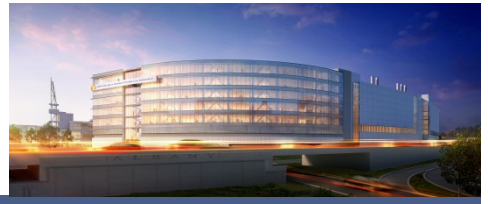
Summary



- The cost component of Moore's law is running into head winds
- The most significant options to continue manufacturing scaling:
  1. EUV still has cost and infrastructure challenges to overcome
  2. The transition to 450mm is projected toward the end of the decade
  3. Chip stacking lacks standards and manufacturing cost issues remain
- Many applications require less aggressive scaling
  - Alternate substrates

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THANK YOU

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